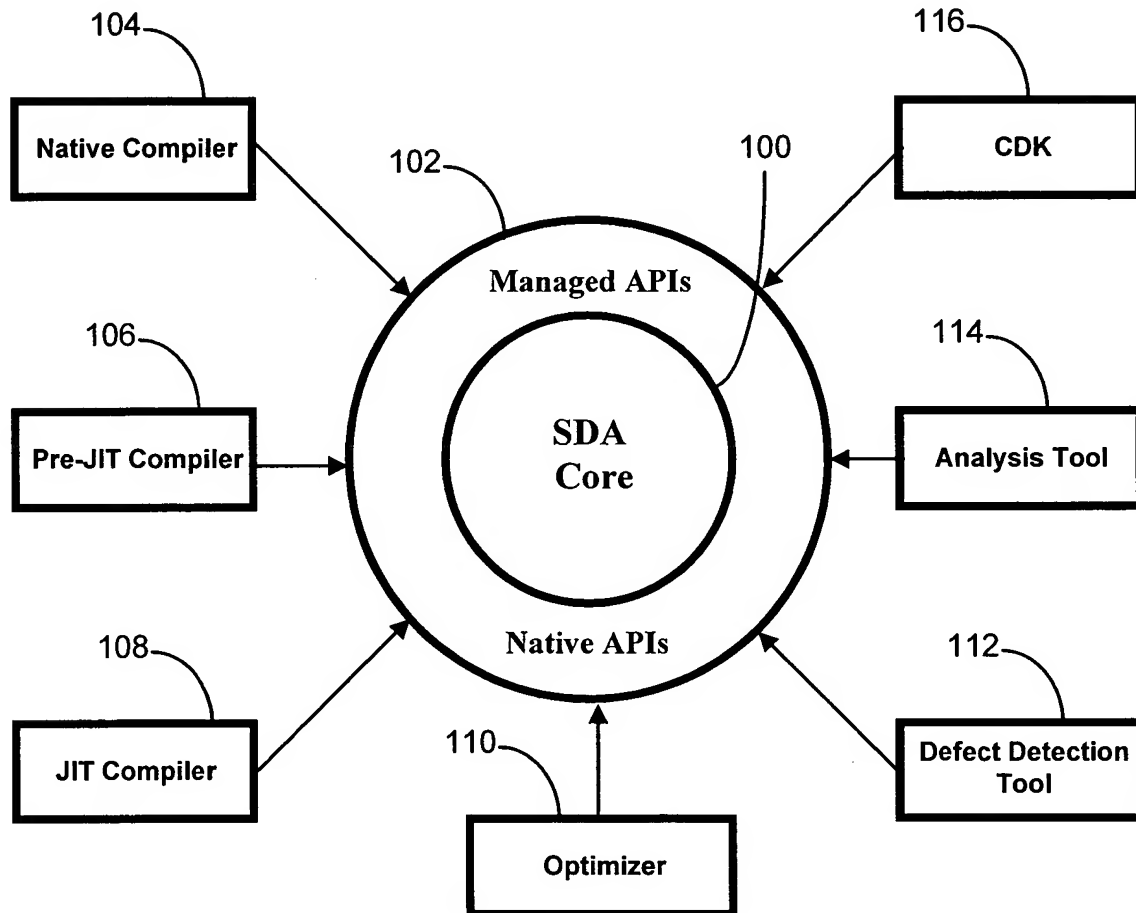


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**FIG. 1**



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FIG. 2(a)

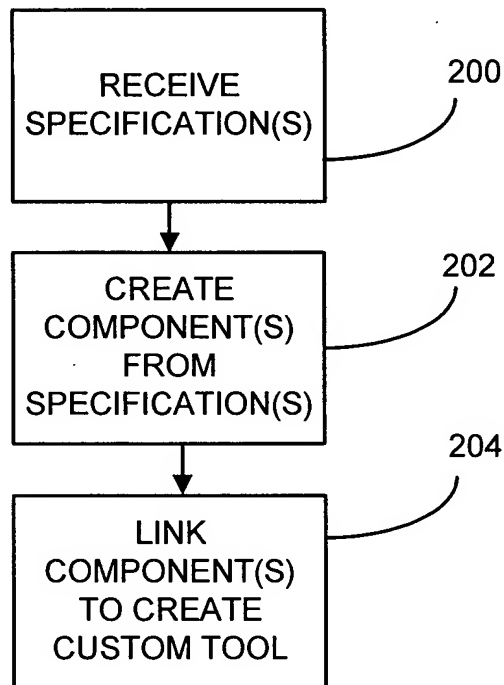
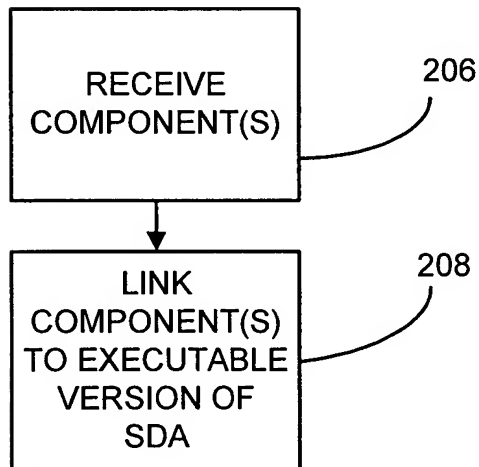
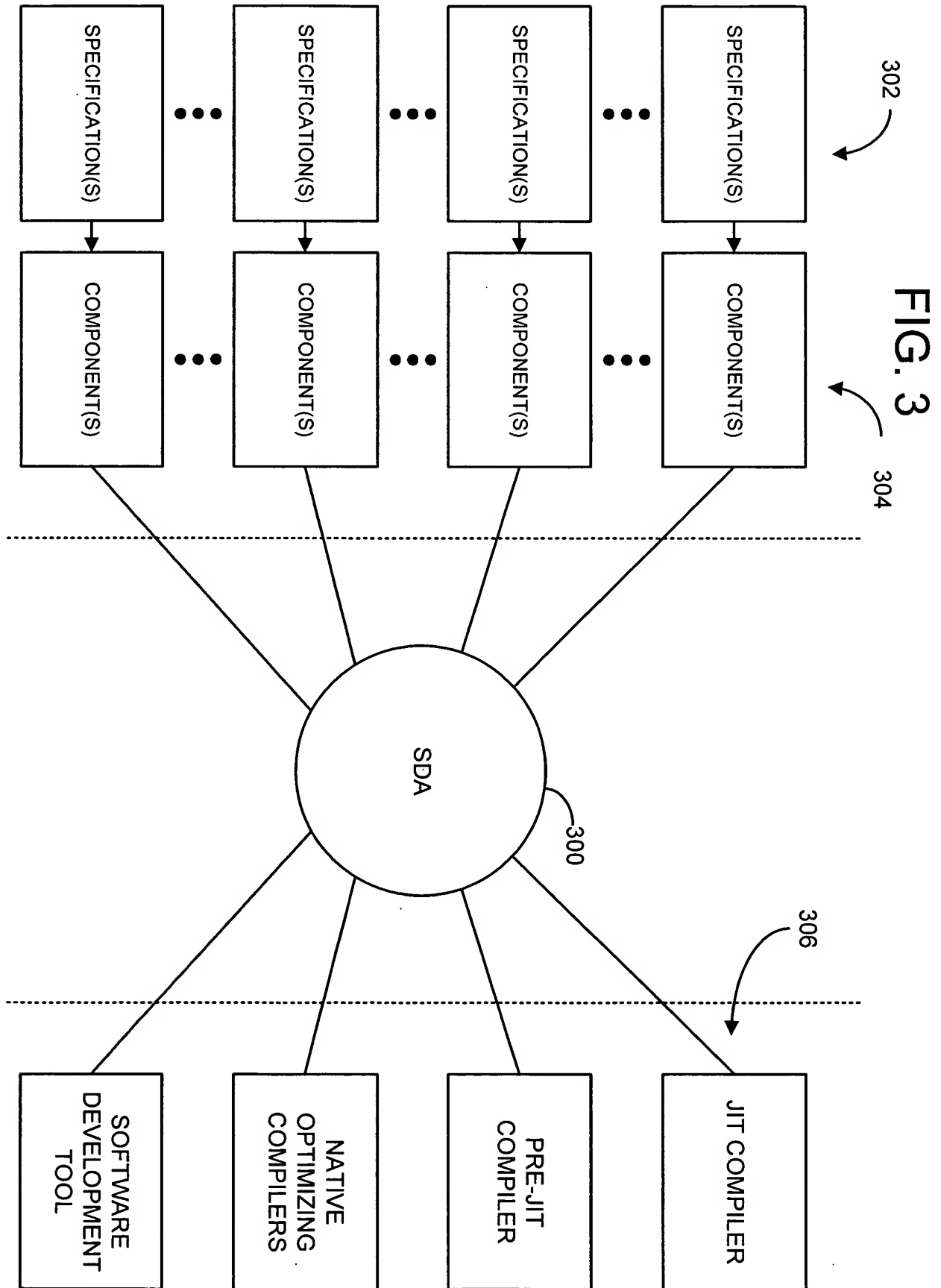


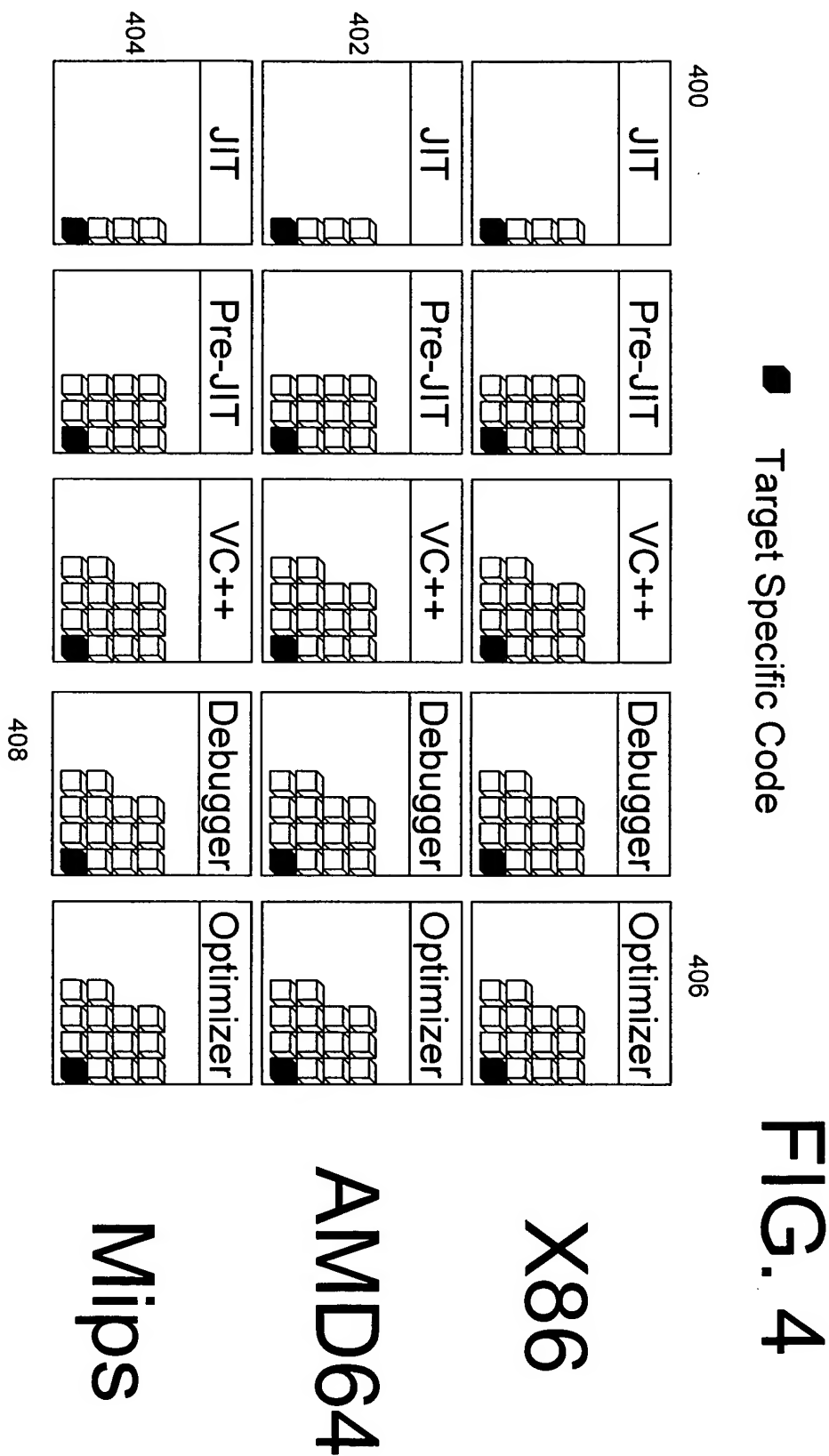
FIG. 2(b)



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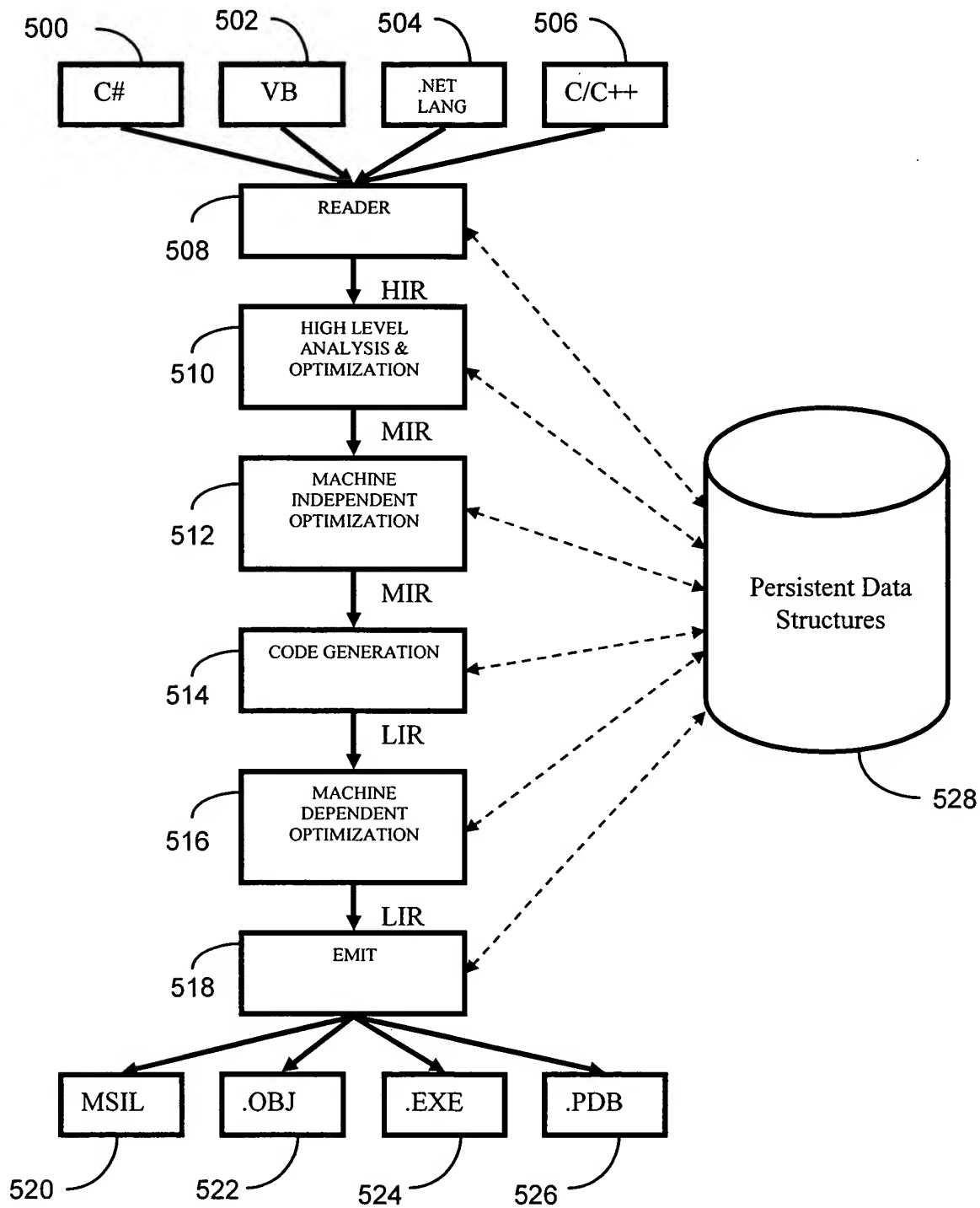




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FIG. 5



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### Source

FIG. 6(a)

```
int foo(int a, int b)
{
    int r;

    if (a < b)
    {
        r = a + 1;
    }
    else
    {
        r = b + 1;
    }

    return r;
}
```

FIG. 6(b)

### Dump of high-level, machine independent IR

	<code>_a.i32, _b.i32</code>	<code>= ENTER _foo</code>	<code>#4</code>
	<code>t107.cond</code>	<code>= CMP(LT) _a.i32, _b.i32</code>	<code>#7</code>
		<code>CBRANCH(LT) t107.cond, L2, L1</code>	<code>#7</code>
<code>L2:</code>			<code>#7</code>
	<code>t108.i32</code>	<code>= ADD _a.i32, 1.i32</code>	<code>#9</code>
	<code>_r.i32</code>	<code>= ASSIGN t108.i32</code>	<code>#9</code>
		<code>GOTO L3</code>	<code>#11</code>
<code>L1:</code>			<code>#7</code>
	<code>t109.i32</code>	<code>= ADD _b.i32, 1.i32</code>	<code>#13</code>
	<code>_r.i32</code>	<code>= ASSIGN t109.i32</code>	<code>#13</code>
		<code>GOTO L3</code>	<code>#11</code>
<code>L3:</code>			<code>#11</code>
		<code>RETURN _r.i32</code>	<code>#16</code>
		<code>GOTO L4</code>	<code>#16</code>
<code>L4:</code>			<code>#16</code>
		<code>EXIT _foo</code>	<code>#17</code>

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## FIG. 6(c)

### Dump of high-level with SSA, machine independent IR

Explicit wiring of SSA graph using definition numbers shown in <#> blue.

```

<1>_a.i32, <2>_b.i32      = ENTER _foo                      #4
<3>t107.cond              = CMP(LT) <1>_a.i32, <2>_b.i32      #7
                           CBRANCH(LT) <3>t107.cond, L2, L1   #7
L2:                        #7
<4>t108.i32               = ADD <1>_a.i32, 1.i32           #9
<5>_r.i32                 = ASSIGN <4>t108.i32              #9
                           GOTO L3                            #11
L1:                        #7
<6>t109.i32               = ADD <2>_b.i32, 1.i32           #13
<7>_r.i32                 = ASSIGN <6>t109.i32              #13
                           GOTO L3                            #11
L3:                        #11
<8>_r.i32                 = PHI <5>_r.i32, <7>_r.i32        #16
                           RETURN <8>_r.i32                 #16
                           GOTO L4                            #16
L4:                        #16
                           EXIT _foo                         #17

```

## FIG. 6(d)

### Dump of low-level, machine dependent IR (target X86)

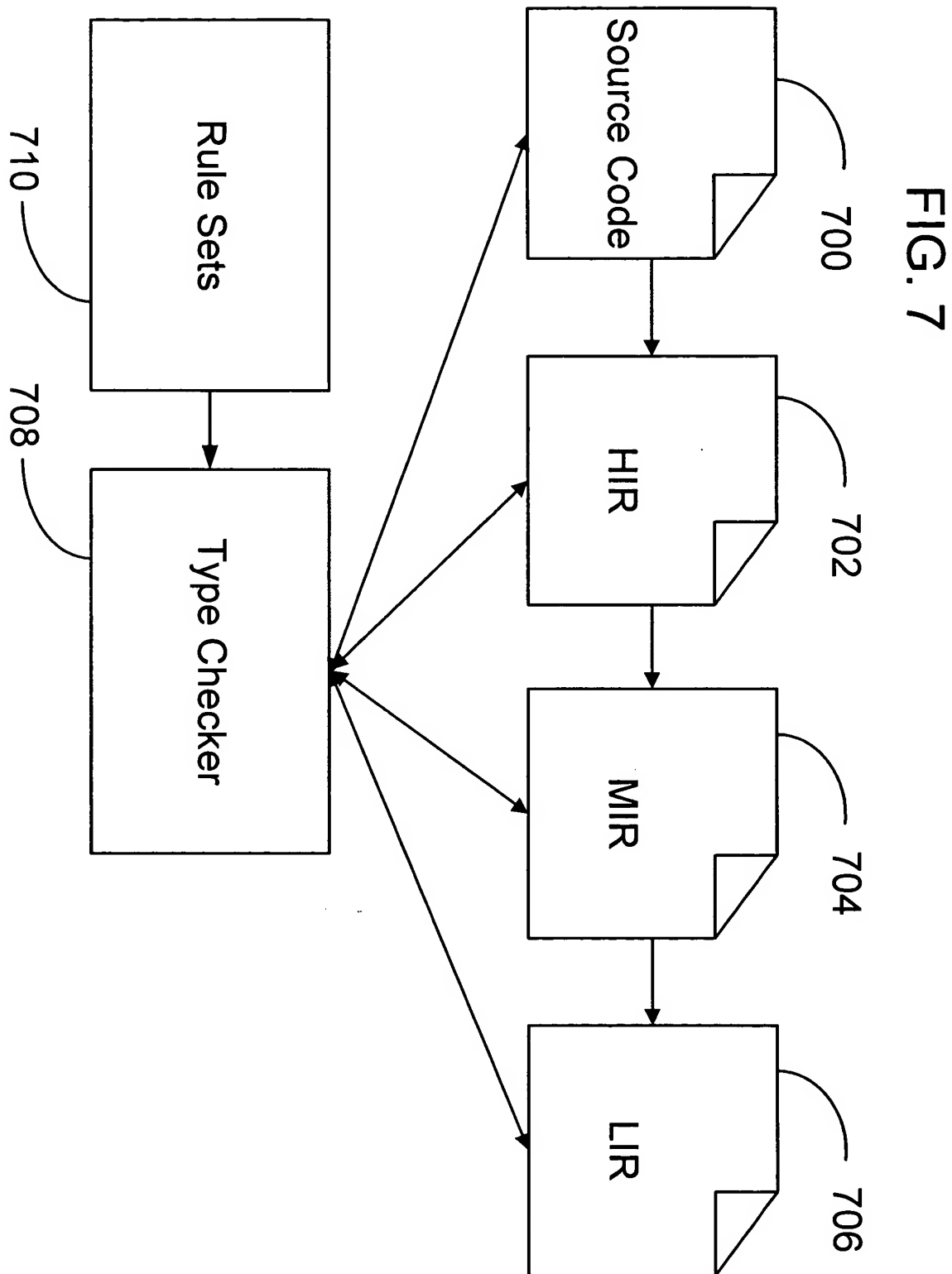
```

_a.i32, _b.i32            = ENTER _foo                      #4
{ESP}                    = push EBP.i32, {ESP}              #4
EBP.i32                   = mov ESP.i32                      #4
ESP.up32->unk, EFLAGS.cc32 = sub ESP.up32->unk, 4.i32        #4
                           PROLOGEND                         #4
t110(EAX).i32             = mov _b[EBP.up32->unk].i32.a32    #7
t107(EFLAGS).cond         = cmp(LT) _a[EBP.up32->unk].i32.a32, t110(EAX).i32 #7
                           jge(GE) t107(EFLAGS).cond, L1     #7
L2:                        #7
tv108-(EAX).i32           = mov 1.i32                       #9
tv108-(EAX).i32, EFLAGS.cc32 = add tv108-(EAX).i32, _a[EBP.up32->unk].i32.a32
#9
_r[EBP.up32->unk].i32.a32 = mov tv108-(EAX).i32             #9
                           jmp L3                             #11
L1:                        #7
tv109-(EAX).i32           = mov 1.i32                       #13
tv109-(EAX).i32, EFLAGS.cc32 = add tv109-(EAX).i32, _b[EBP.up32->unk].i32.a32
#13
_r[EBP.up32->unk].i32.a32 = mov tv109-(EAX).i32             #13
L3:                        #11
t113(EAX).i32             = mov _r[EBP.up32->unk].i32.a32    #16
L4:                        #16
                           EPILOGSTART                      #17
ESP.i32                   = mov EBP.i32                      #17
EBP.i32, {ESP}            = pop {ESP}                        #17
{ESP}                     = ret {ESP}                        #17
                           EXIT _foo, t113(EAX).i32          #17

```

Replacement Sheet

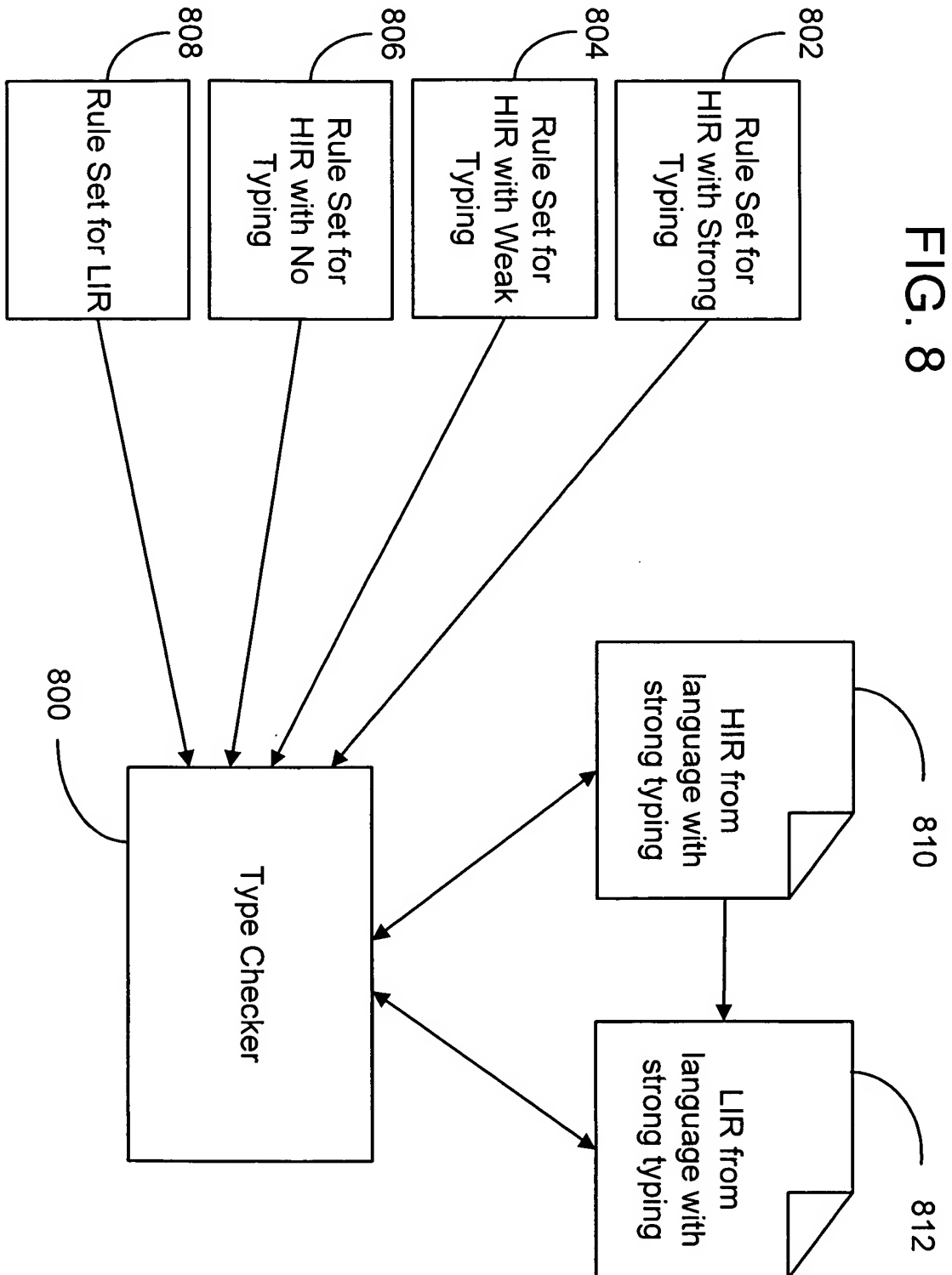
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FIG. 9

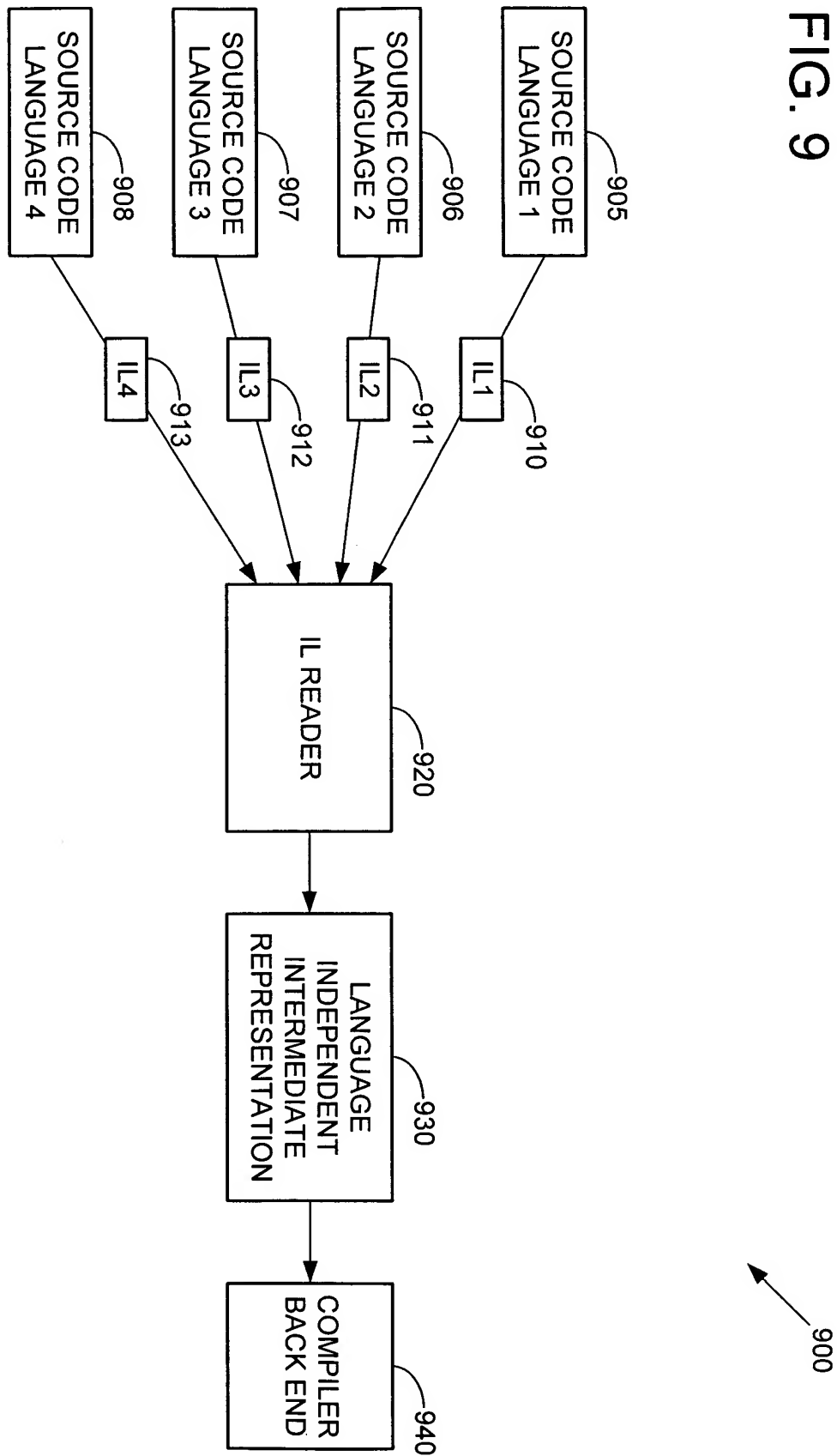


FIG. 10A

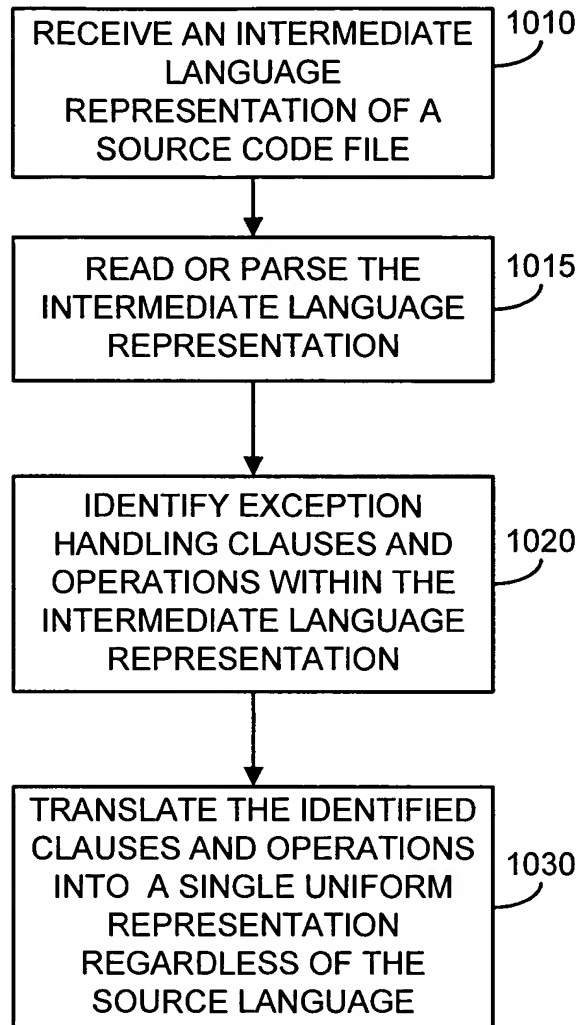
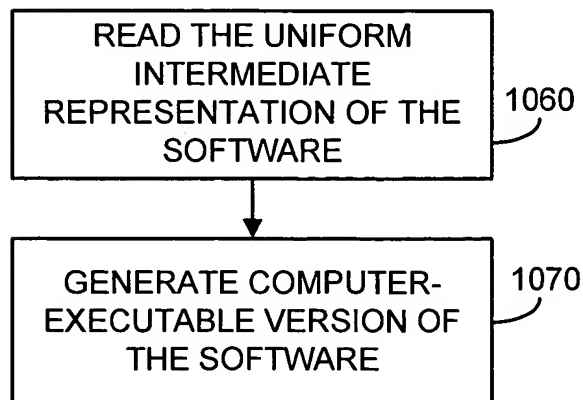


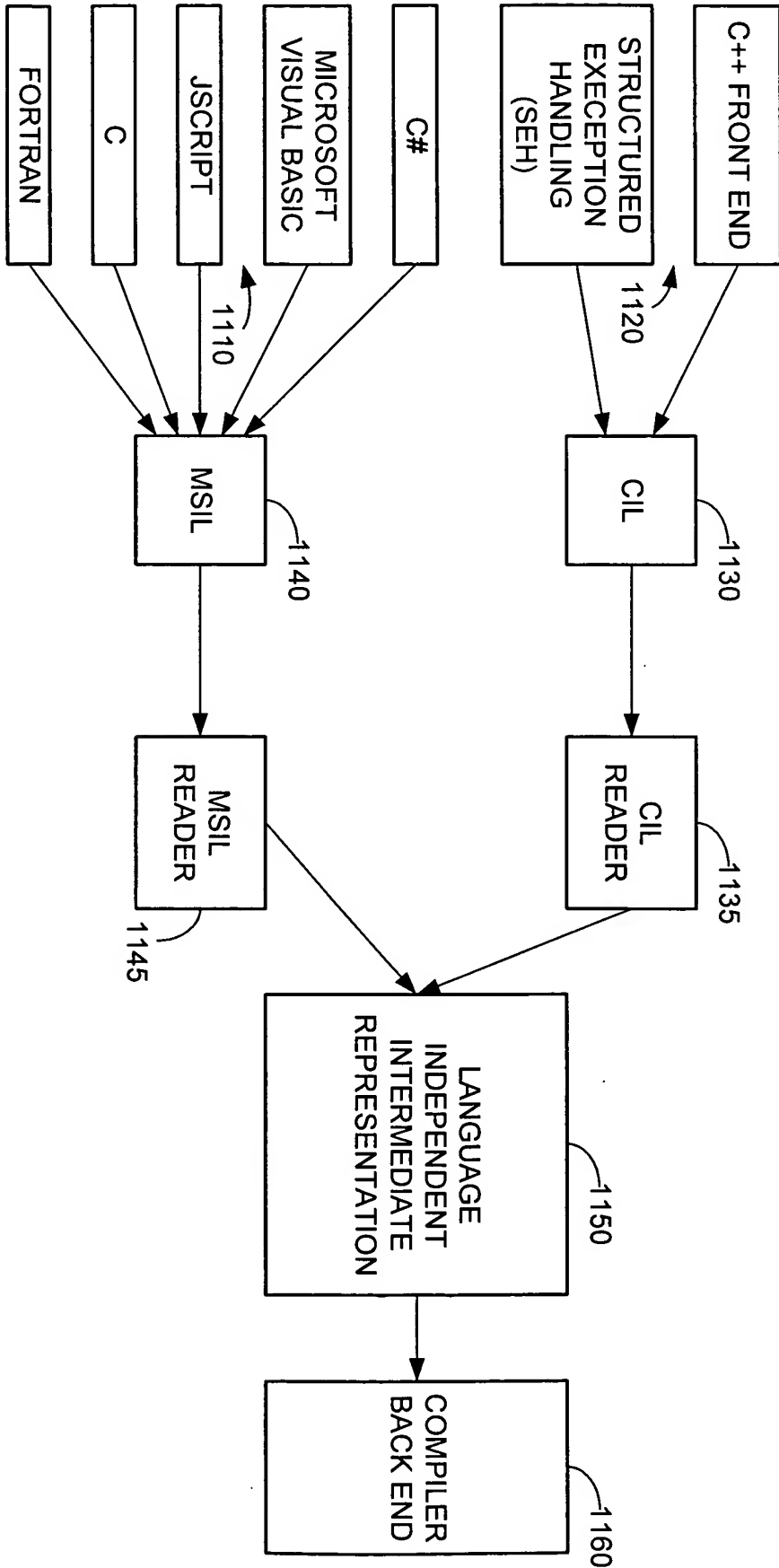
FIG. 10B



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FIG. 11



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FIG. 12

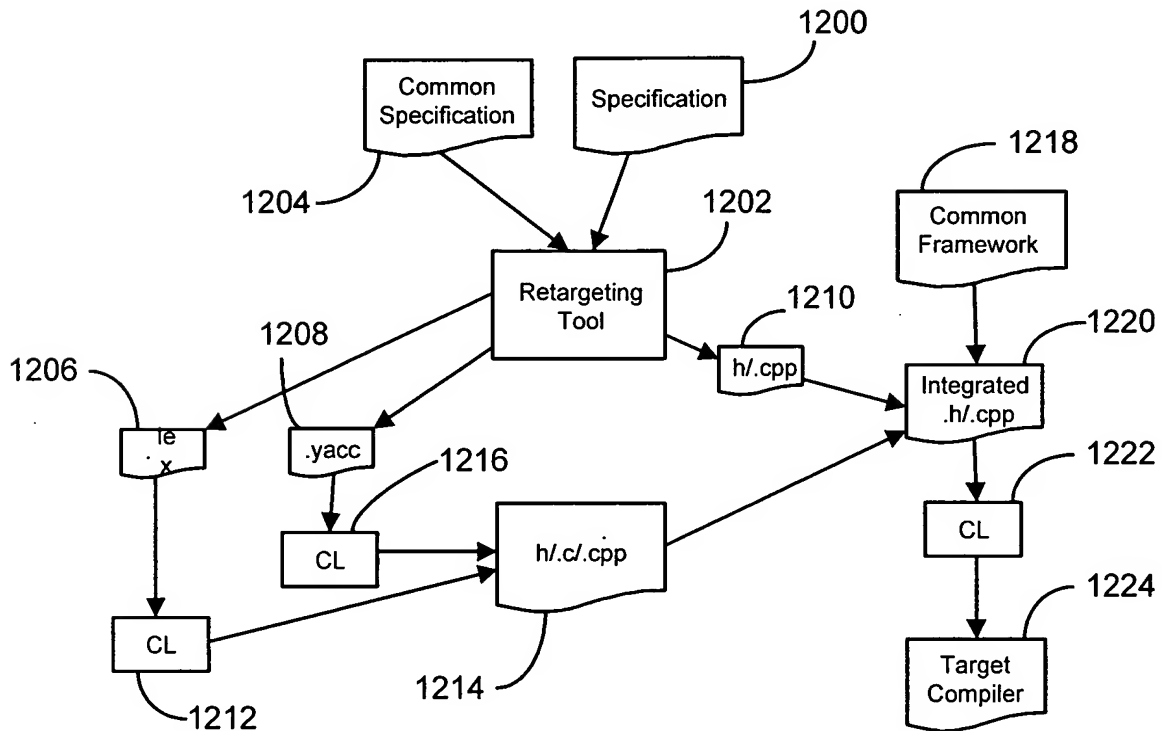
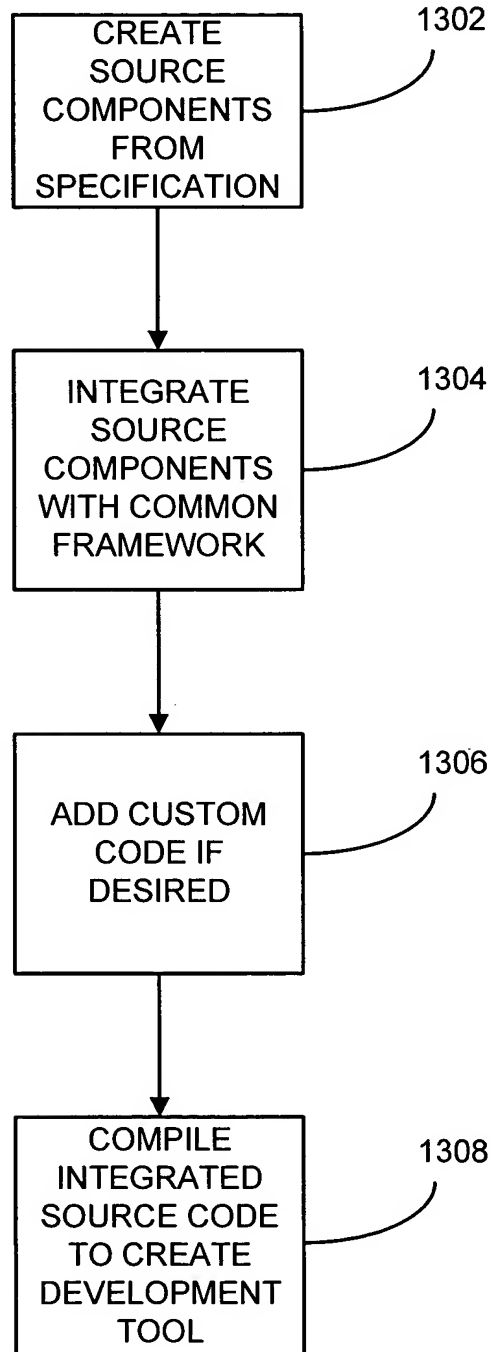


FIG. 13



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**FIG. 14(a)**

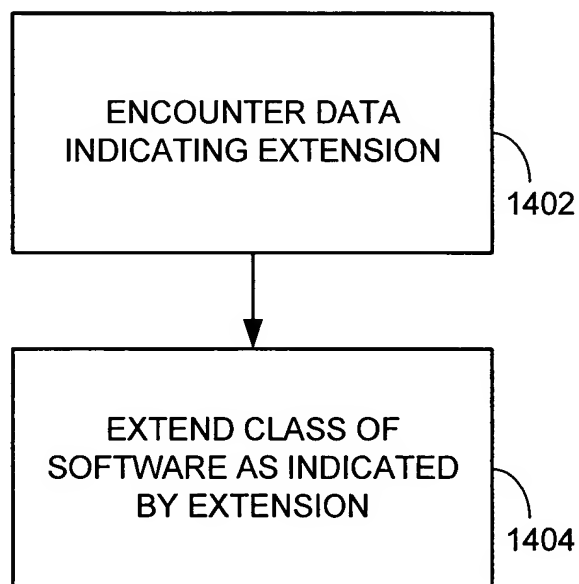


FIG. 14(b)

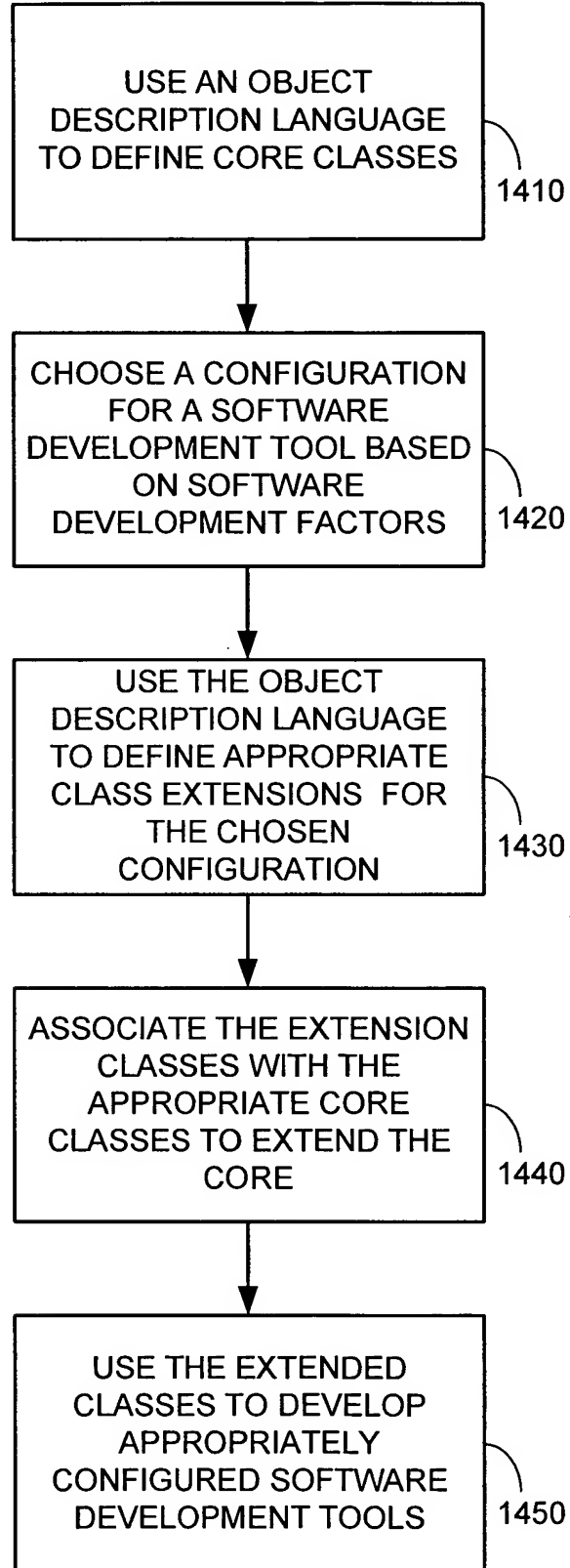




FIG. 15(a)

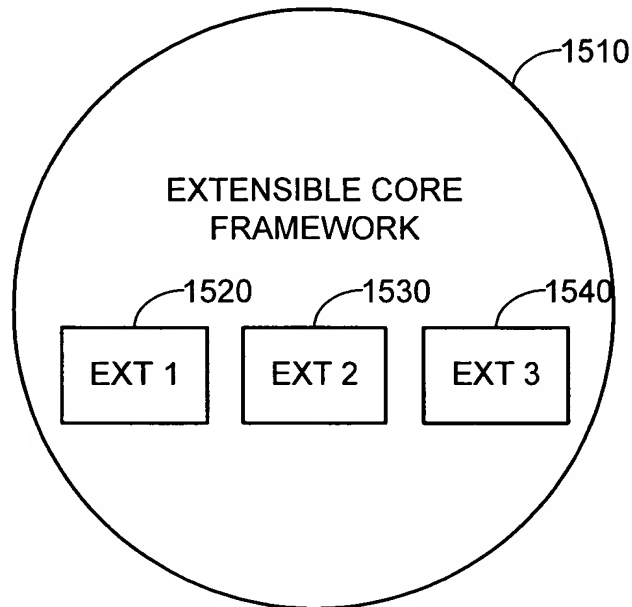
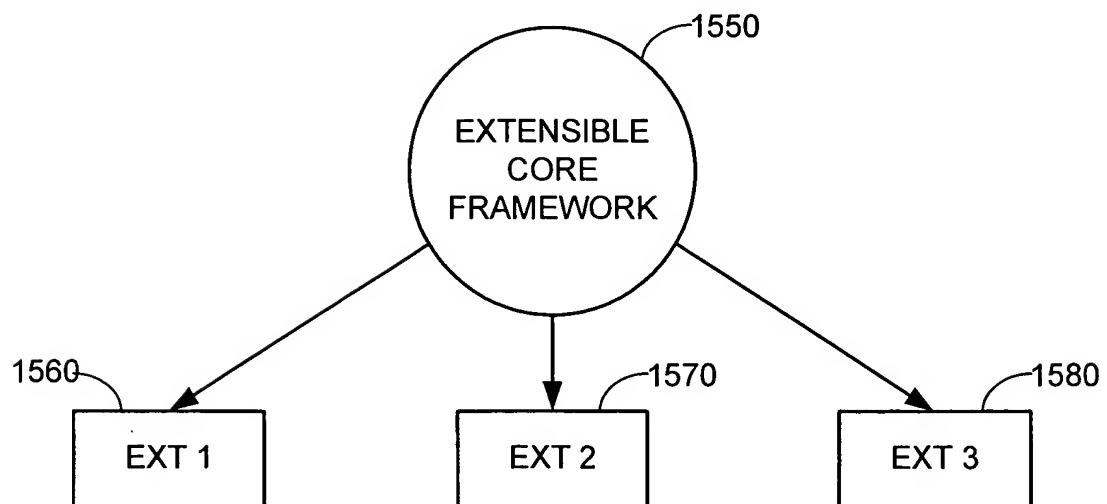


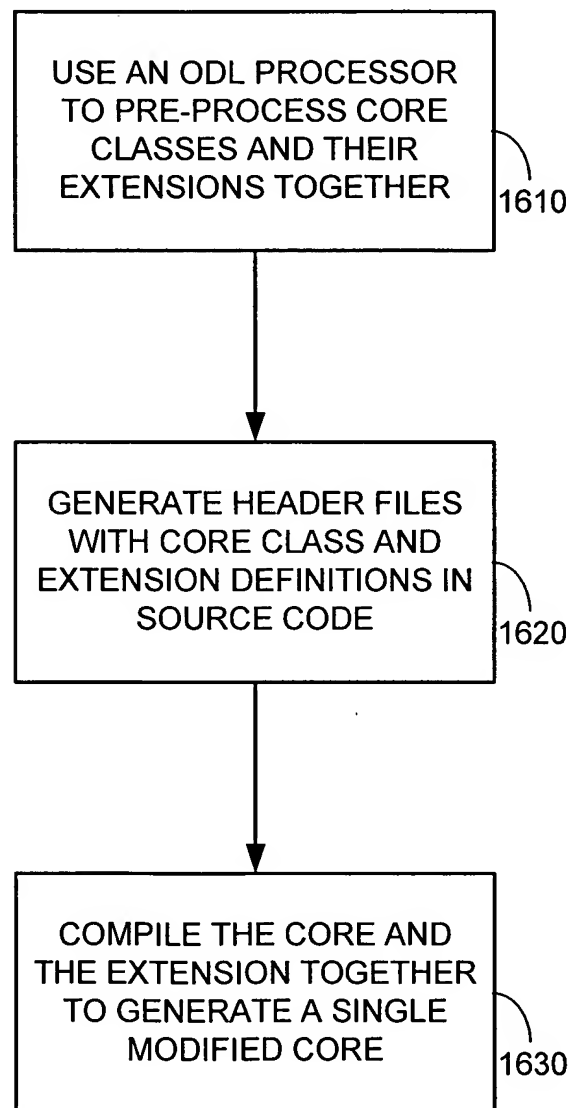
FIG. 15(b)



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FIG. 16



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FIG. 17

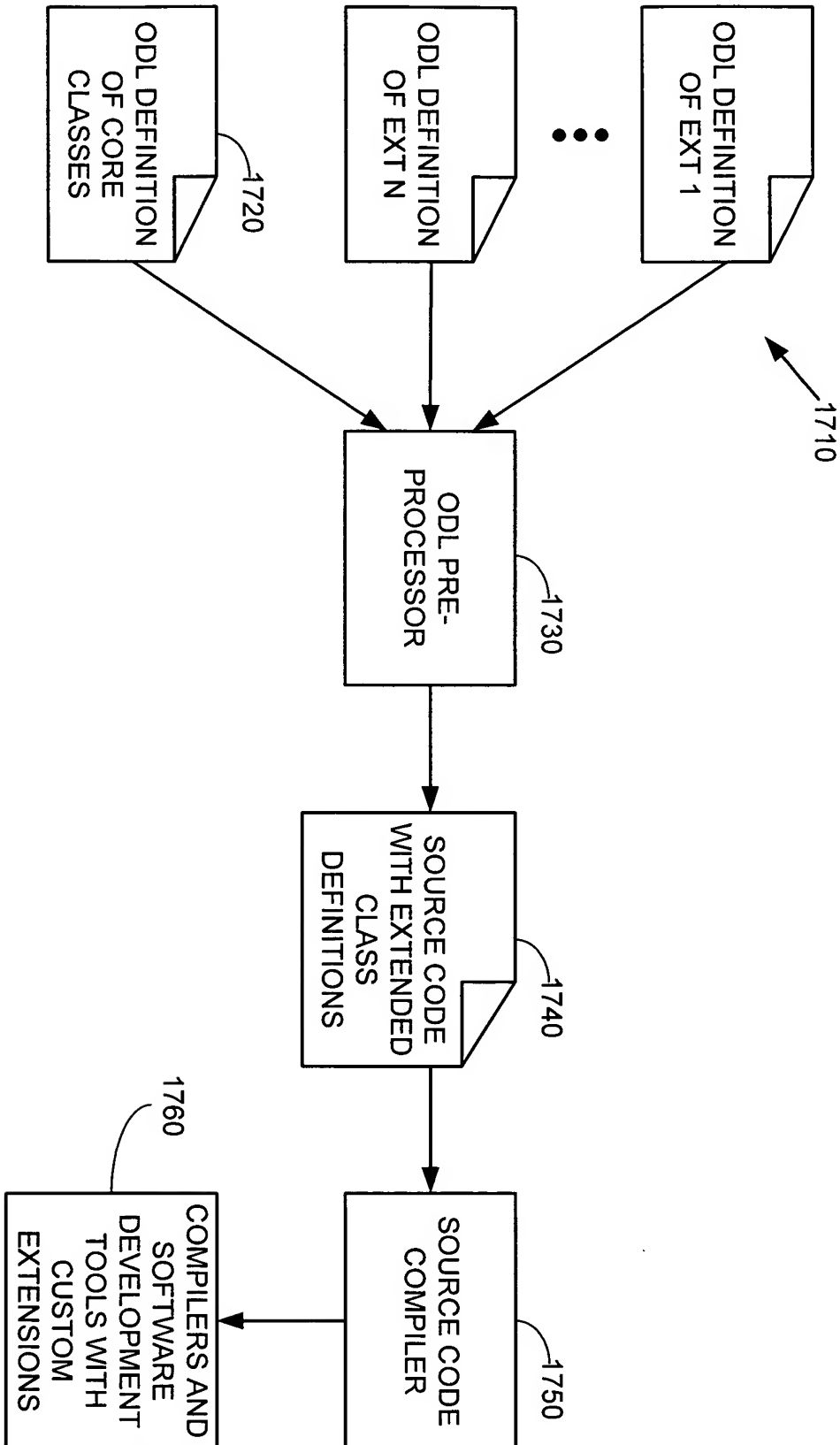
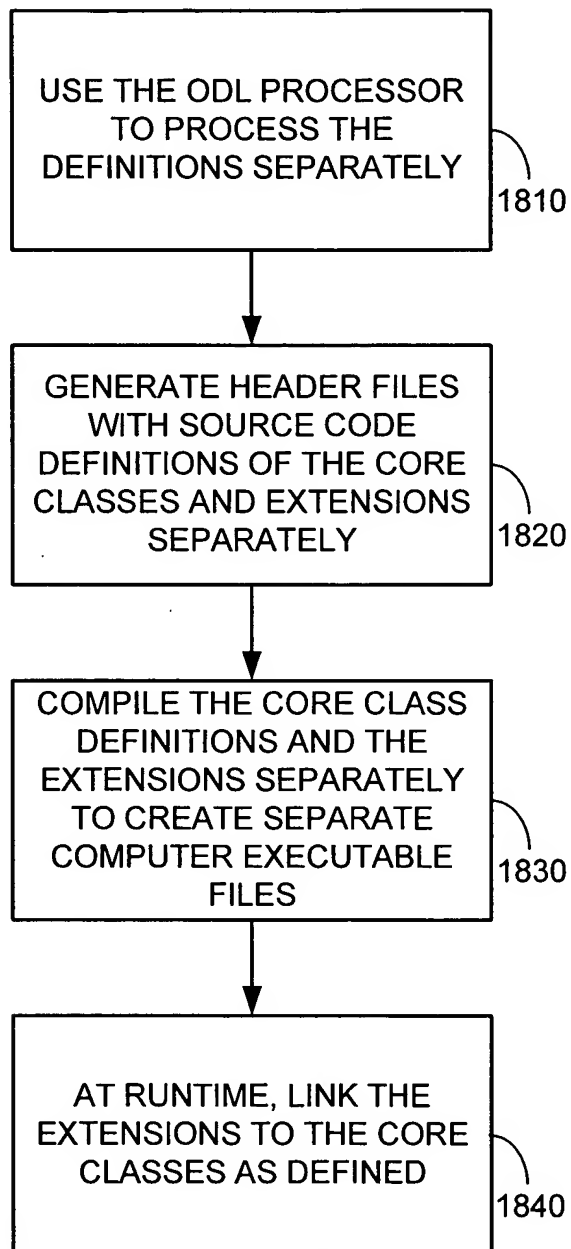
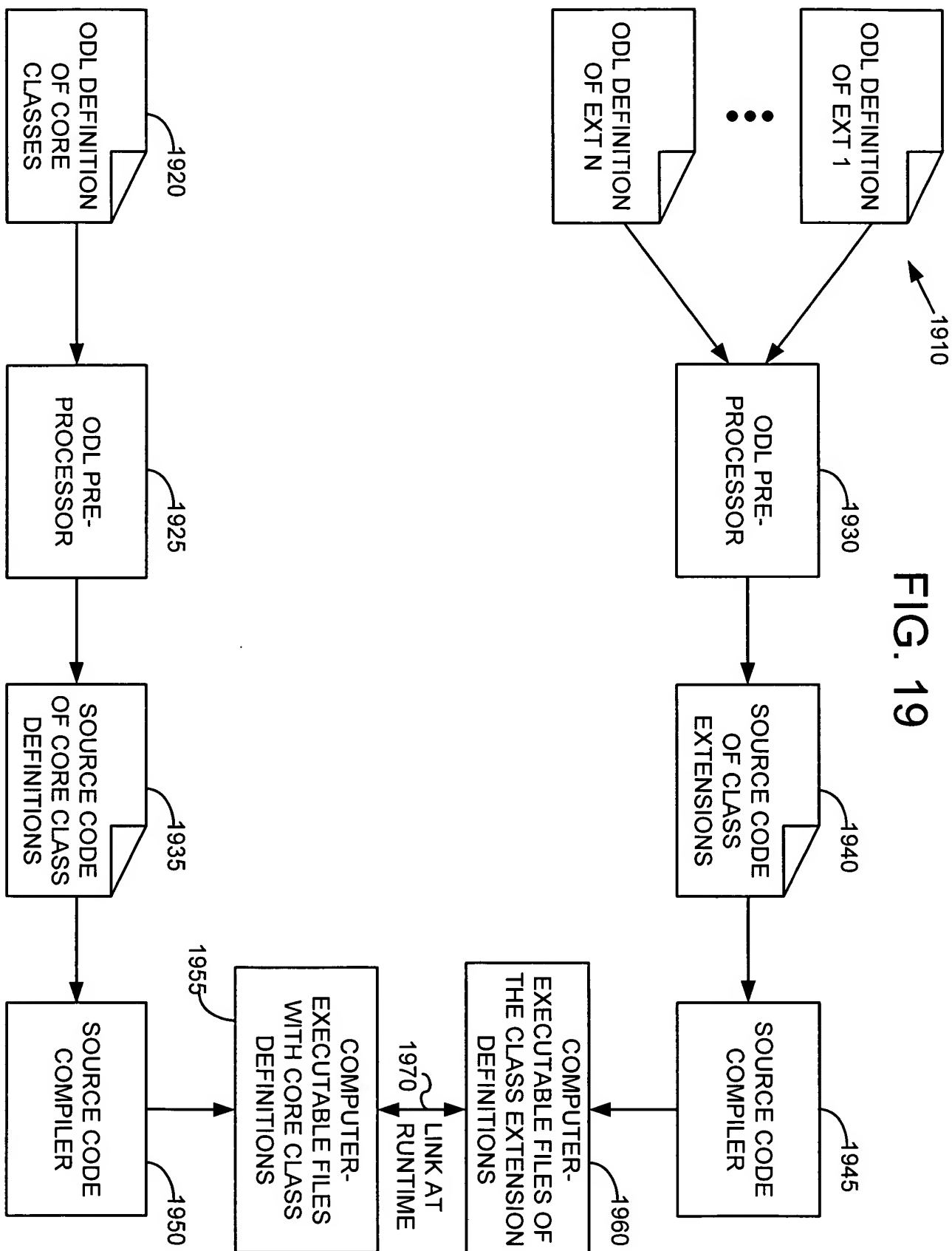


FIG. 18



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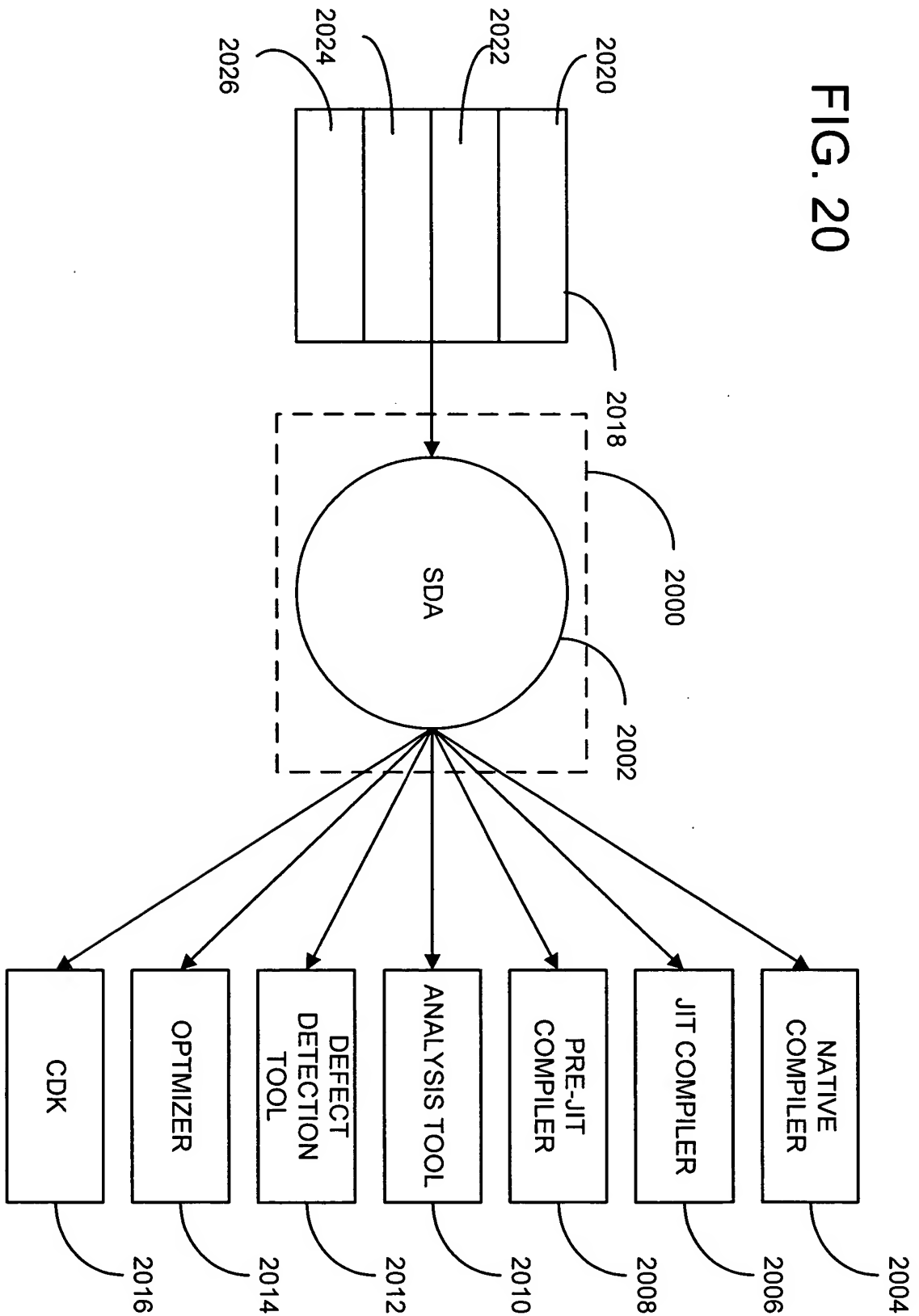
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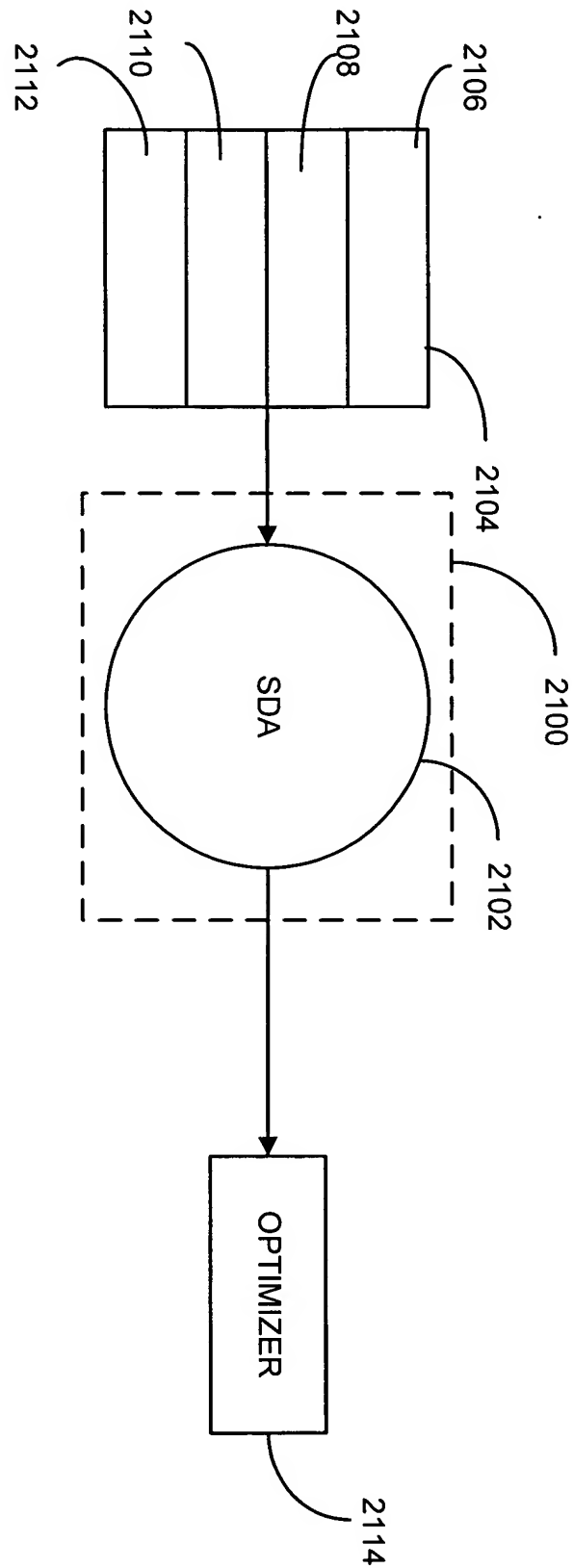
FIG. 20



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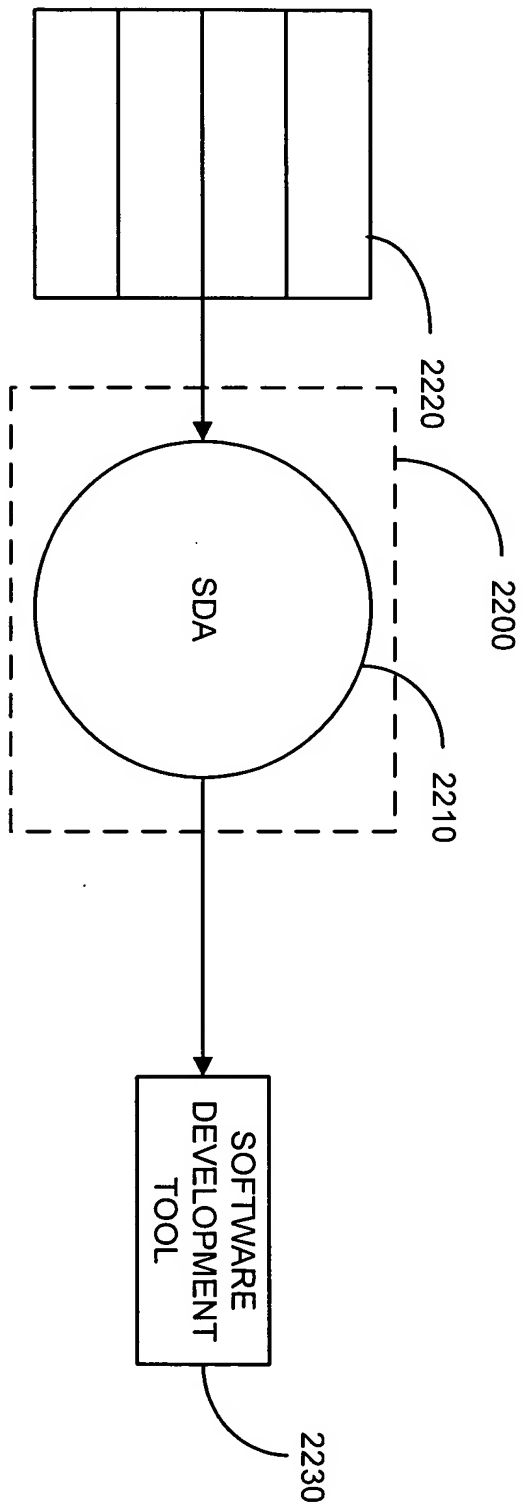
FIG. 21



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FIG. 22

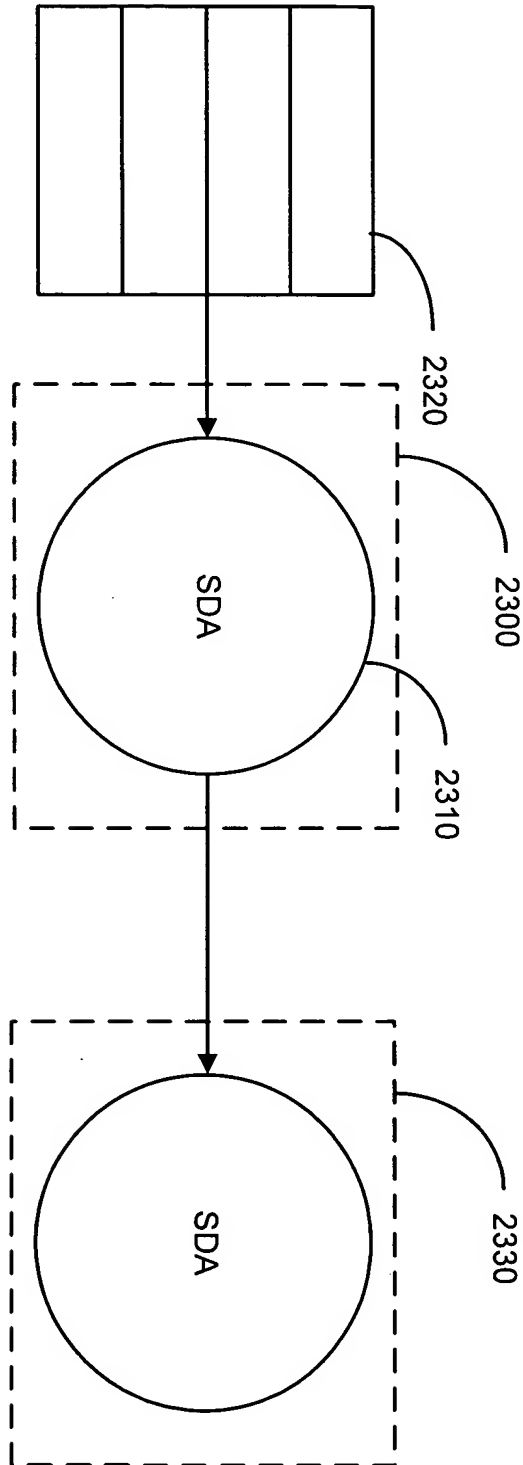




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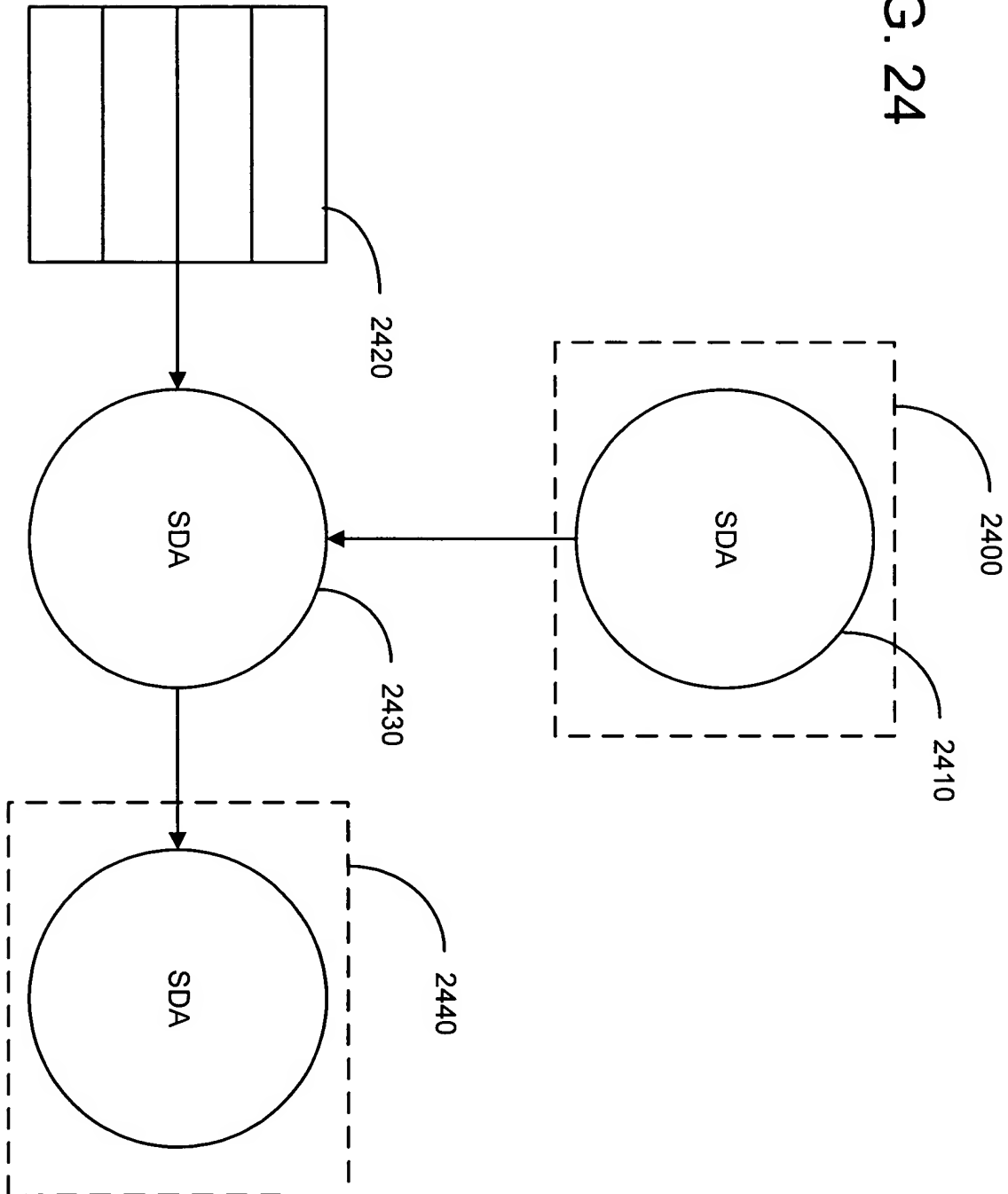
FIG. 23



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FIG. 24



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